TFT LCD Approval Specification

MODEL NO.: V562D1–L02

Customer: _____

Approved by:_____

Note

Approved By	TV Head Division
	LY Chen

Reviewed By	QA Dept.	Product Development Div.
	Hsin-nan Chen	WT Lin

Prepared By	LCD TV Marketing and Product Management Div.	
	CY Chang	Michell Tsung

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver 2.0	Mar. 9,'07	All	All	Approval Specification is first issued.
Ver 2.1	Jul.25,'07	5	1.5	Modify the value of Horizontal(H) and Vertical(V).
		14	4.2.3	Add Note (4)、(5).
		16	5.1	Modify CN1:S14B-PH-SM4-TB(D)(LF).
				Modify CN2:S12B-PH-SM4-TB(D)(LF).
		19	6.4	Modify CN1:S14B-PH-SM4-TB(D)(LF).
				Modify CN2:S12B-PH-SM4-TB(D)(LF).
		28	8.2	Modify Center Luminance of White to Typ.=450 nits and Min.=400 nits.
		36	12	Add screw hole section drawing.
Ver 2.2	Sep.25,'07	6	2.1	Modify Max. of Operating Ambient Temperature to 45 ºC.
		6	2.1	Modify Note (2) Surface temperature of display area should be less than or equal to 70 ºC.
		11	4.2.1	Modify the value of Lamp Current.
		11	4.2.2	Modify the value of Power Consumption and Power Supply Current.
		12	4.2.2	
		12	4.2.2	Modify Note (4) IL = 5.5 ~ 6.5mA rms.
		28	8.1	Modify Note (6) average lamp current 6.3mA.
		28	8.2	Modify the value of Lamp Current.
		30	8.2	Modify Cross Talk from 4% to 2%.
		31	8.2	Modify Note (5).
				Modify Note (7).
Ver 2.3	JUL.9,'09	12	4.2.2	Add note
		15	4.2.3	Modify INVERTER INTERTFACE CHARACTERISTICS.
		25	7.1	Remove Note (1)
		28	7.4	Remove Note (3)
		34	10.1	Modify module label.
		35	11.2	Remove Drier.
		37	12	Modify rear drawing form no sensor hole to two sensor hole
		38	12	Modify rear drawing form no sensor hole to two sensor hole

1. GENERAL DESCRIPTION

1.1. OVERVIEW

V562D1-L02 is a 56" Thin-Film-Transistor Liquid-Crystal (TFT-LCD) module with one 32-CCFL backlight unit and 4 ports Single-DVI utilization. This module supports 3840 x 2160 Quad Full High Definition (QFHD) TV format and can display 16.7M colors (8-bit). The inverter module for backlight is also built-in.

1.2. FEATURES

Ultra Wide Viewing Angle (176(H)/176(V) for CR>30)

High Brightness (450 nits)

High Contrast Ratio (1200:1)

Ultra Fast Response Time (Gray to gray average 6.5 ms)

High Color Saturation (NTSC 75%)

QFHD (3840 x 2160 pixels) Resolution

4 ports Single-DVI (Digital Visual Interface)

RoHS Compliance

1.3. APPLICATION

Luxurious Living Room TVs

Public Display

Home Theater

Satellite Communication

Medical Analyses/ Instruction

Security and Monitoring

Industrial Design

3D Display

Digital Museum

Multi-Media Display

1.4. GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1244.16 (H) x 699.84 (V) (56.2" diagonal)	mm	
Bezel Opening Area	1252.1 (H) x 707.8 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.108 (H) x 0.324 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Hard coating 3H Low reflection coating< 2% reflection	-	(1)

Note (1) The specifications of the surface treatment are temporarily for this phase. CMO reserves the rights to change this feature.

1.5. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	1309	1309.5	1310.2	mm	
	Vertical(V)	766.5	767	767.7	mm	
	Depth(D)	57.2	58.5	59.8	mm	To PCB cover
	Depth(D)	61.9	63.2	64.5	mm	To inverter cover
Weight		23000	23500	24000	g	

2. ABSOLUTE MAXIMUM RATING

2.1. ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+55	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	45	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	30	G	(3), (5)
		Z axis	-	30	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

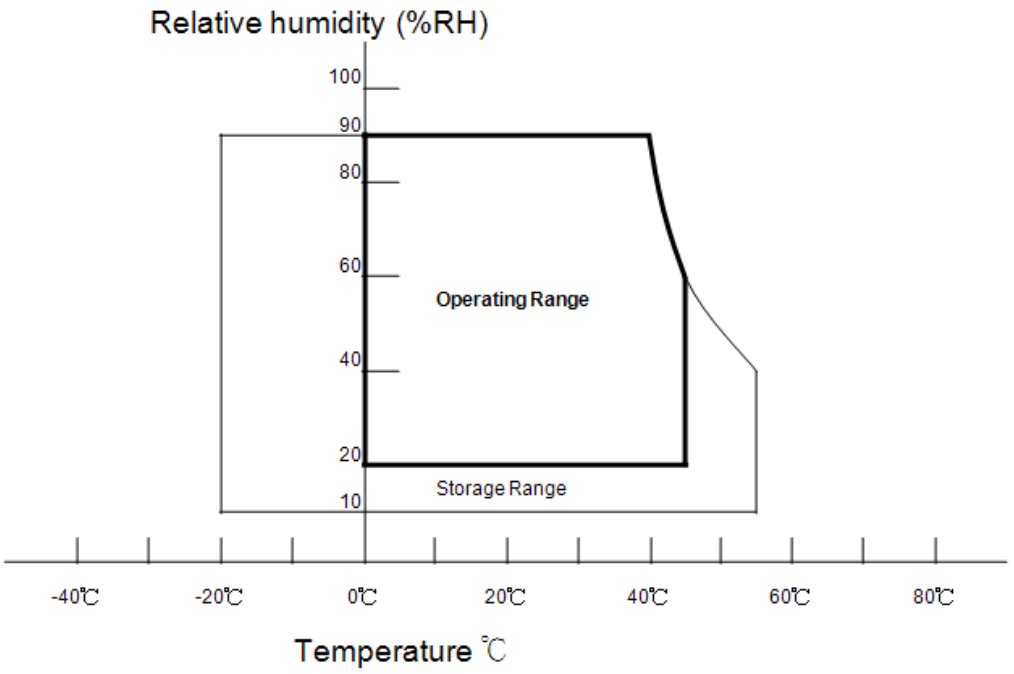
Note (1) Temperature and relative humidity range is shown in the figure below.
(a) 90 %RH Max. (Ta ≦ 40 ºC).
(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 70 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 70 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2. RATINGS OF IMAGE STICKING

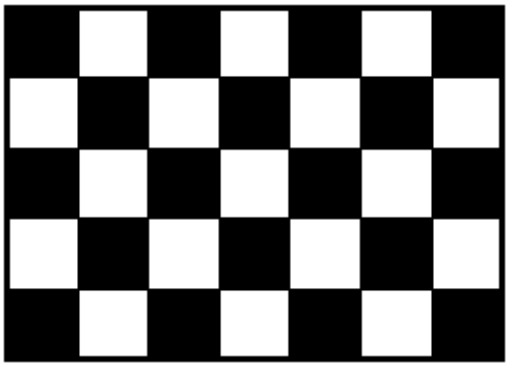
Item	Symbol	Value	Unit	Note
Room Temperature Image Sticking	RT IS	Invisibility	6% ND (%)	(1)(3)
High Temperature Image Sticking	HT IS	Invisibility	6% ND (%)	(2)(3)

Note (1) Room temperature image sticking test is at 25±3 °C environment and fix the pattern A (checker pattern) for 12 hours.

Note (2) High temperature image sticking test is at 50±3 °C environment and fix the pattern A for 12 hours.

Note (3) Inspection condition is at pattern B (128grade) after 5 mins from pattern A.

A. Pattern A (checker pattern)



B. Pattern B (128grade)

3. ELECTRICAL MAXIMUM RATINGS

3.1. TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC1}	-0.3	20	V	
	V_{CC2}	-0.3	6	V	
DVI Termination Supply Voltage	AVcc		4.0	V	(2)
DVI Signal Voltage on any pin	-	-0.5	4.0	V	
DVI Differential Mode Signal Voltage on any pin	-	-0.5	4.0	V	
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under normal operating conditions.

Note (2) The maximum ratings of the DVI are specified in the DVI specification of DDWG.

3.2. BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (2), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

4. ELECTRICAL CHARACTERISTICS

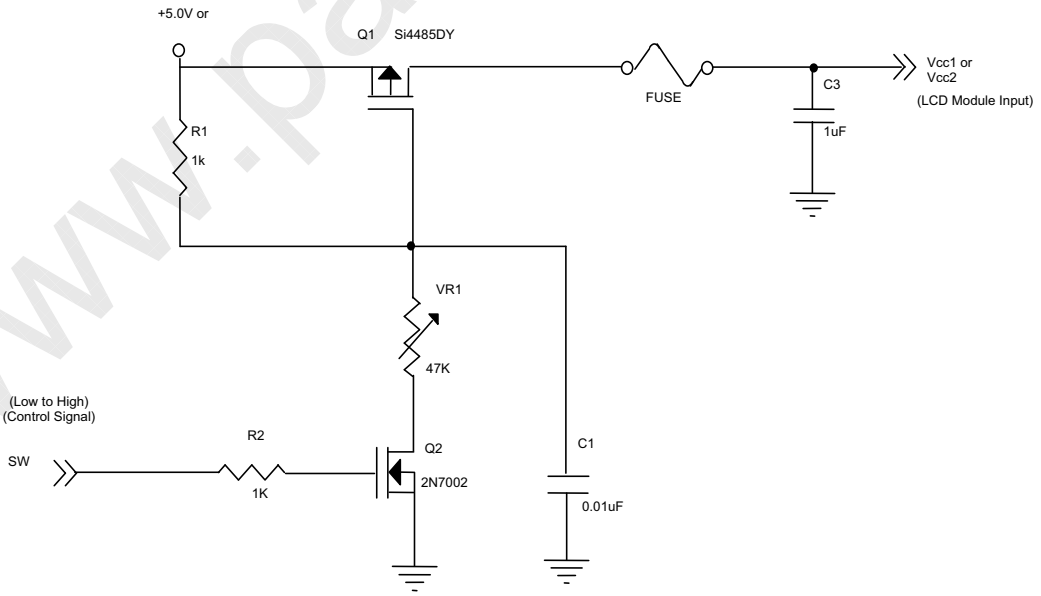
4.1. TFT LCD MODULE

Ta = 25 ± 2 ºC

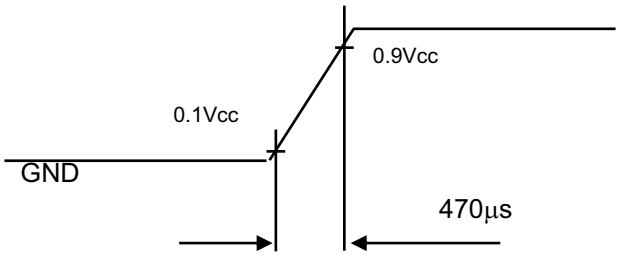
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC1}	17.1	18	18.9	V	(1)
		V_{CC2}	4.5	5	5.5	V	
Power Supply Ripple Voltage		V_{RP1}	-	-	400	mV	
		V_{RP2}			200	mV	
Rush Current		I_{RUSH1}	-	-	4.5	A	(2)
		I_{RUSH2}	-	-	14	A	
Power Supply Current	White	I_{CC1}	-	1.9	2.5	A	(3)
	Black		-	0.7	-	A	
	Vertical Stripe		-	1.5	-	A	
	White	I_{CC2}	-	5.4	-	A	
	Black		-	4.9	-	A	
	Vertical Stripe		-	5.5		A	
	V-Stripe-2column			7.2	9	A	
DVI Interface	Differential Input Voltage Single Ended Amplitude	V	100	-	800	mV	(4) (5)
	Receiver Resistor	R_T	95	100	105	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement conditions:



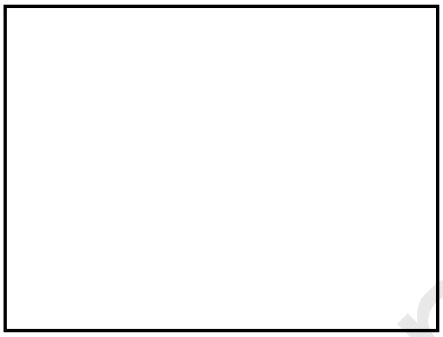
Vcc rising time is at least 470μs



Note (3) The specified power supply current is under the conditions at Vcc1 = 18 V, Vcc2 = 5 V, Ta = 25 ± 2 °C,

f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

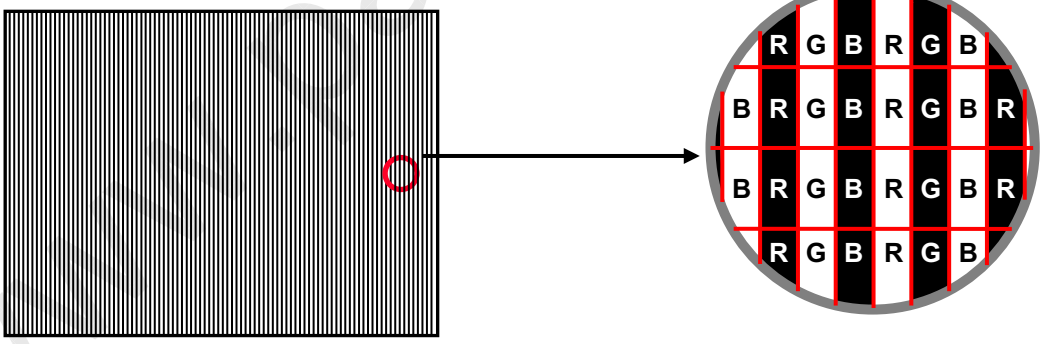


Active Area

b. Black Pattern

Active Area

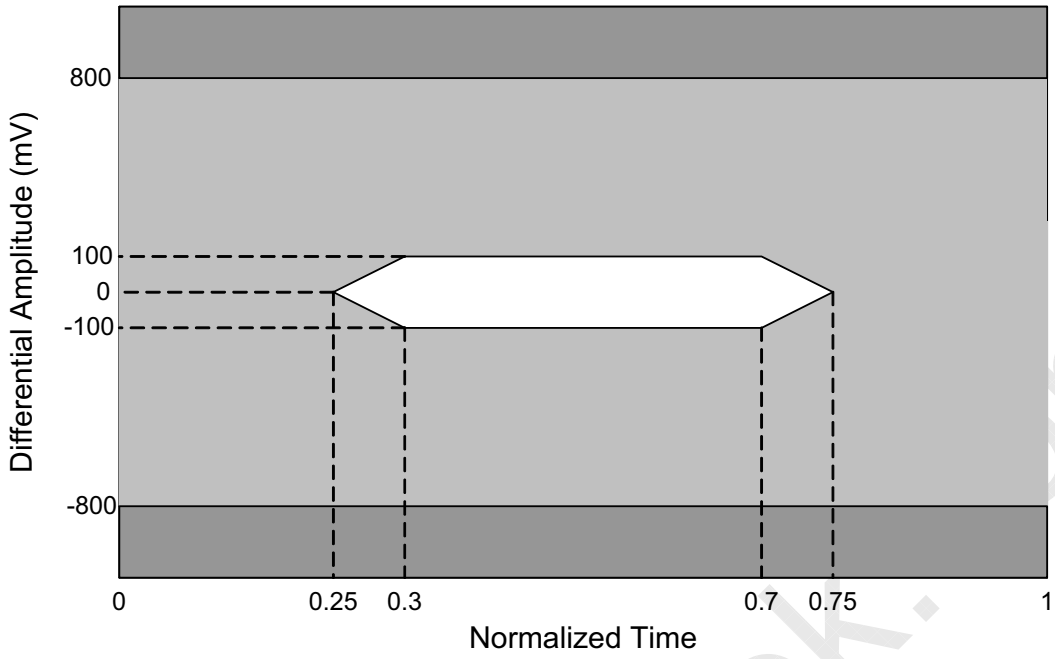
c. Vertical Stripe Pattern



Active Area

Note (4) The electrical characteristics of DVI are specified in the DVI specification of DDWG.

Note (5) The receiver shall reproduce a test data stream, with pixel error rate 10^{-9}, when presented with input amplitude illustrate by the eye diagram.



Absolute Eye Diagram Mask at TP3

4.2. BACKLIGHT UNIT

4.2.1. CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS

(Ta=25±2℃)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Voltage	VW	-	1728	-	VRMS	IL =5.7mA
Lamp Current	IL	5.5	6.0	6.5	mARMS	(1)
Lamp Starting Voltage	VS	-	-	2550	VRMS	(2), Ta = 0 ºC
		-	-	2350	VRMS	(2), Ta = 25 ºC
Operating Frequency	Fo	40	60	80	KHz	(3)
Lamp Life Time	LBL	-	50000	-	Hrs	(4)

4.2.2. INVERTER CHARACTERISTICS

(Ta=25±2℃)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	315	330	W	(5), I_L = 6.0mA
Power Supply Voltage	V_{BL}	22.8	24.0	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	13.13	13.75	A	Non Dimming
Input Ripple Noise	-	-	-	500	mV_{P-P}	V_{BL}=22.8V
Oscillating Frequency	F_W	47	50	53	kHz	
Dimming frequency	F_B	150	160	180	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup.

Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 5.5 ~ 6.5mA rms.

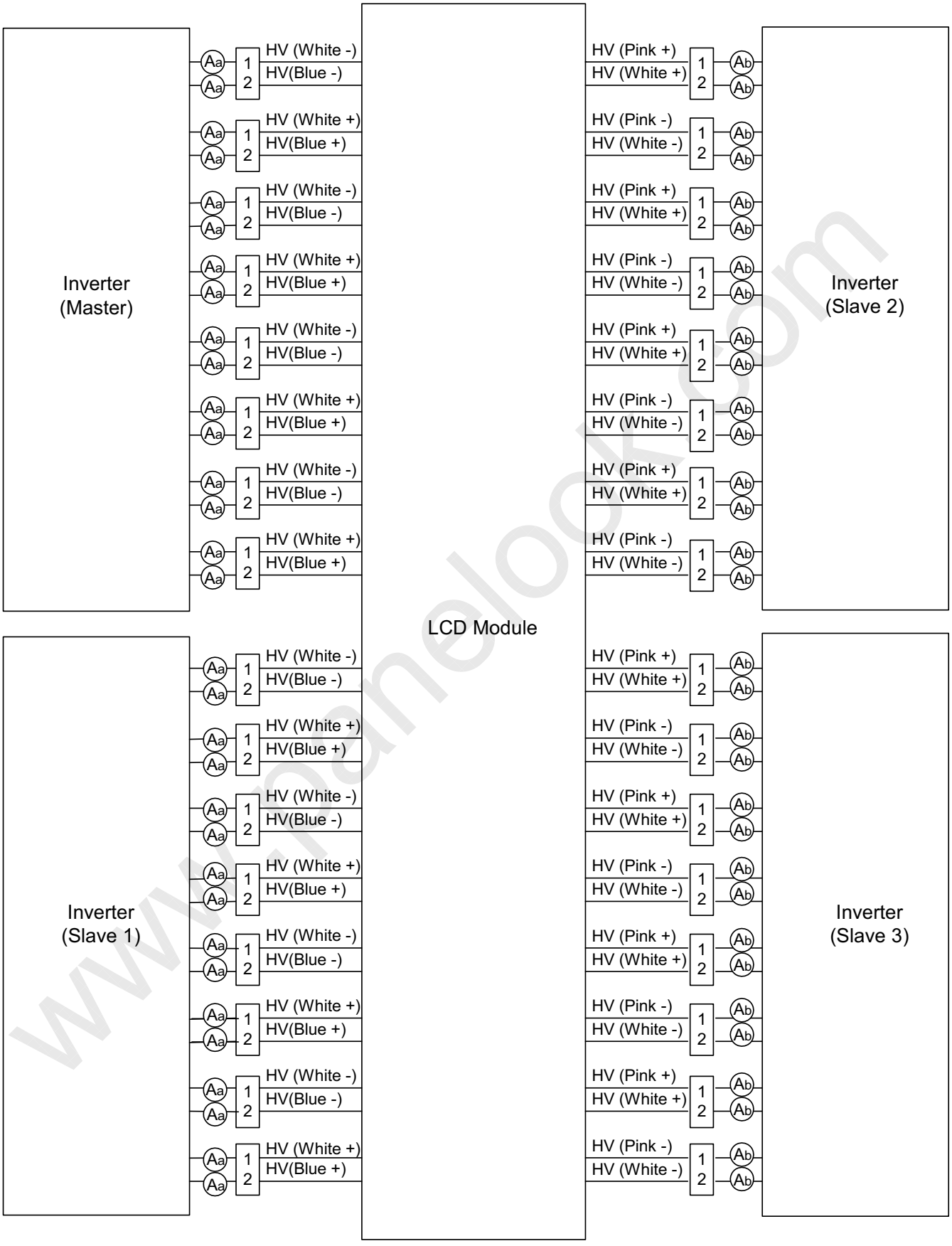
Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 56" backlight unit under input voltage 24V, average lamp current 6.3 mA and lighting 30 minutes later.

Note (7) The voltage difference of power supply voltage (V_{BL}) between Master and Slave board could not over 1V.

CHI MEI OPTOELECTRONICS CORP.

Issue Date:JUL.9.2009
Model No.: V562D1-L02
Approval



4.2.3. INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	3.15	3.3	3.45	V	Note (5)
	MIN			—	0	—	V	minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	duty on
	LO			0	—	0.8	V	duty off
VBL Rising Time		Tr1	—	30	—	50	ms	
VBL Falling Time		Tf1	—	30	—	50	ms	
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
PWM Delay Time		T_{PWM}	—	100	—	300	mS	
BLON Delay Time		T_{on}	—	300	—	500	ms	
BLON Off Time		T_{off}	—	300	—	500	ms	

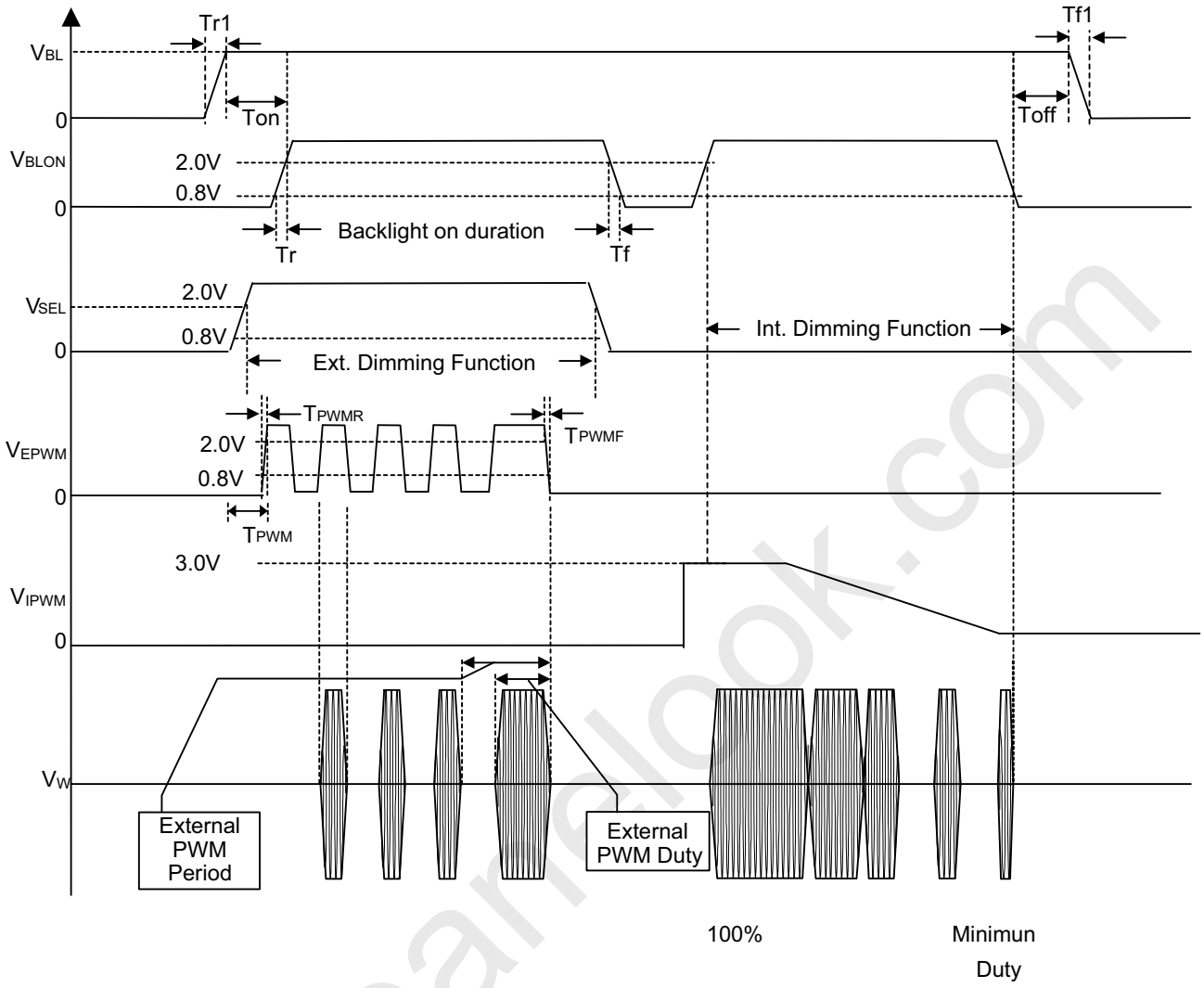
Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.

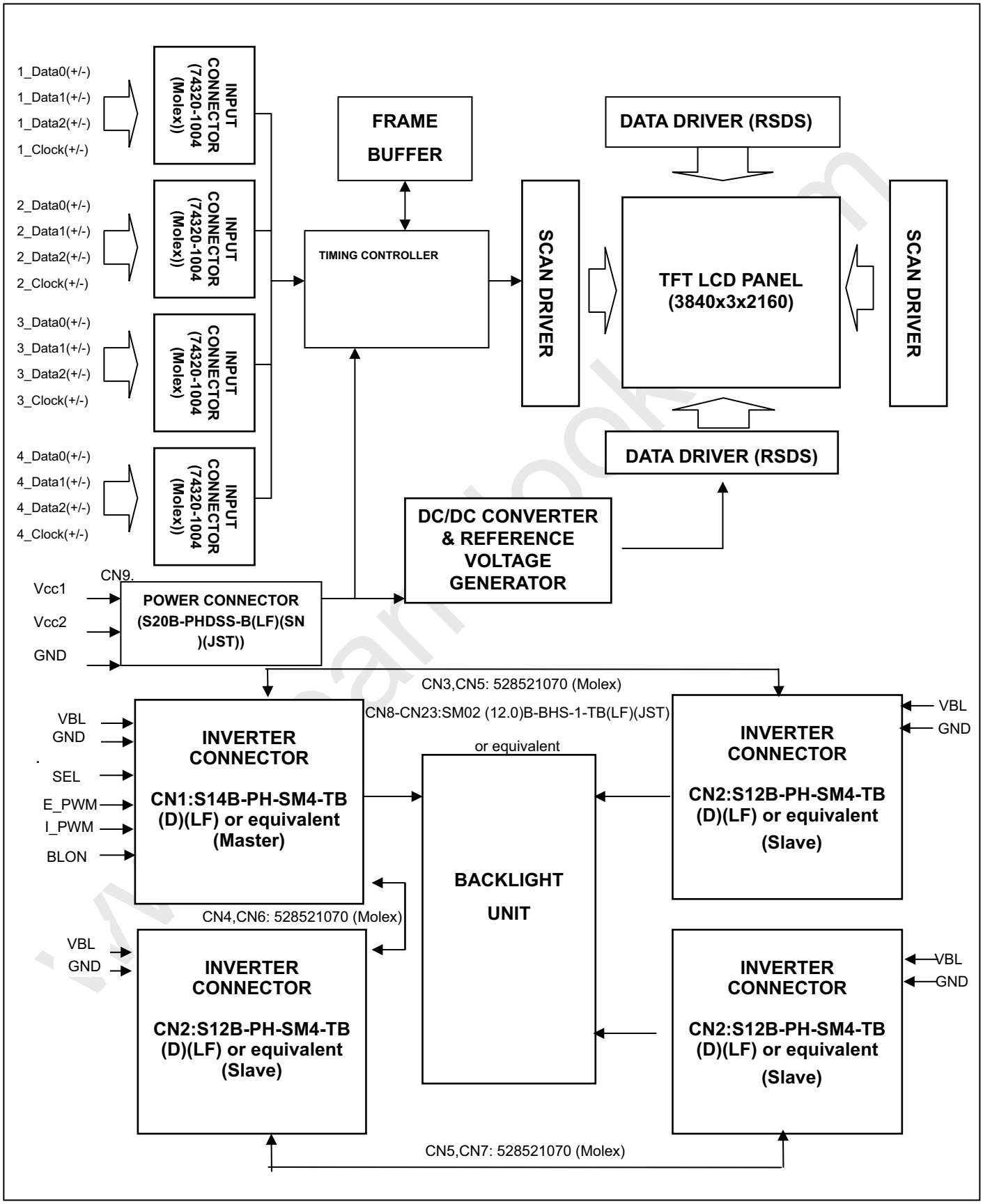
Note (4) Abnormal operation may occur if these maximum values of control signal are exceeded.

Note (5) The range of V_{IPWM} for dimming brightness should be constrained from 0V to 2.85V (i.e., 2.85V is the start dimming point) except the Max. value of V_{IPWM} mentioned here is only for the maximum brightness useful. In other words, 2.85V~3.15V is not suggested for using to prevent from possibly abnormal phenomenon.



5. BLOCK DIAGRAM

5.1. TFT LCD MODULE



6. LCD INPUT TERMINAL PIN ASSIGNMENT

6.1. TFT LCD MODULE DVI INPUT

CN3, CN4, CN5, CN6 Connector Pin Assignment

Pin	Signal Assignment	Pin	Signal Assignment	Pin	Signal Assignment
1	T.M.D.S Data2-	9	T.M.D.S Data1-	17	T.M.D.S Data0-
2	T.M.D.S Data2+	10	T.M.D.S Data1+	18	T.M.D.S Data0+
3	T.M.D.S Data2/4 shield	11	T.M.D.S Data1/3 shield	19	T.M.D.S Data0/5 shield
4	T.M.D.S Data4-	12	T.M.D.S Data3-	20	T.M.D.S Data5-
5	T.M.D.S Data4+	13	T.M.D.S Data3+	21	T.M.D.S Data5+
6	DDC Clock	14	+5V Power	22	T.M.D.S Clock shield
7	DDC Data	15	Ground(for +5V)	23	T.M.D.S Clock+
8	No Connect	16	Hot Plug Detect	24	T.M.D.S Clock-
C1	No Connect	C2	No Connect	C3	No Connect
C4	No Connect	C5	No Connect		

Note (1) CN3, CN4, CN5, CN6 Connector part no.: 74320-1004 (Molex) or equivalent.

Note (2) The DVI pin assignment is specified in the DVI specification of DDWG.

6.2. TFT LCD MODULE POWER INPUT

CN9 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VIN	+18.0V power supply	
2	VIN	+18.0V power supply	
3	V5VC	+5.0V power supply	
4	V5VC	+5.0V power supply	
5	V5VC	+5.0V power supply	
6	NC	No Connection	
7	V5VC	+5.0V power supply	
8	NC	No Connection	
9	V5VC	+5.0V power supply	
10	NC	No Connection	
11	GND	Ground	
12	NC	No Connection	
13	GND	Ground	
14	NC	No Connection	
15	GND	Ground	
16	ODSEL	ODSEL	(3)
17	GND	Ground	
18	GND	Ground	
19	GND	Ground	
20	GND	Ground	

Note (1) CN9 connector part no.: S20B-PHDSS-B(LF)(SN), JST(日本壓著端子),德通端子 or equivalent.

Note (2) CN10 is just only for CMO internal testing.

Note (3) ODSEL (Overdrive Lookup Table Selection). The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL	Note
L	Lookup table was optimized for 60Hz frame rate.
H	Lookup table was optimized for 50Hz frame rate.

Note (4) "L" and "H" operation in (3) could follow "CMOS Interface" in Section 4.1.

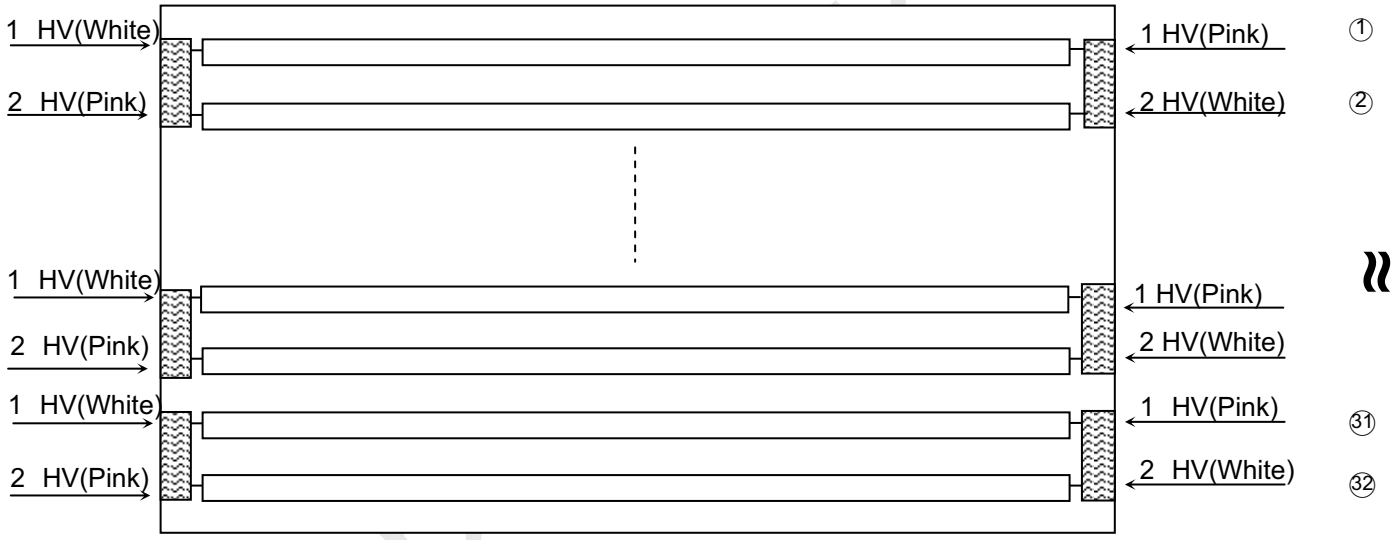
6.3. BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN8-CN23: BHR-04VS-1 (JST).

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-04VS-1, manufactured by JST and the mating header on inverter part number is SM02 (12.0) B-BHS-1-TB (LF).



6.4. INVERTER UNIT

CN1 (Master, Header): S14B-PH-SM4-TB (D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
12	E_PWM	External PWM control signal E_PWM should be connected to ground when internal PWM was selected (SEL = Low).
13	I_PWM	Internal PWM Control Signal I_PWM should be connected to ground when external PWM was selected (SEL = High).
14	BLON	Backlight on/off control

CN2 (Slave, Header): S12B-PH-SM4-TB (D)(LF)(JST) or equivalent

Pin No.	Symbol	Description
1	VBL	+24V_{DC} power input
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN8-CN15 (Master, Header), CN16-CN23 (Slave, Header): SM02 (12.0) B-BHS-1-TB (LF)(JST) or equivalent

Pin No.	Symbol	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage

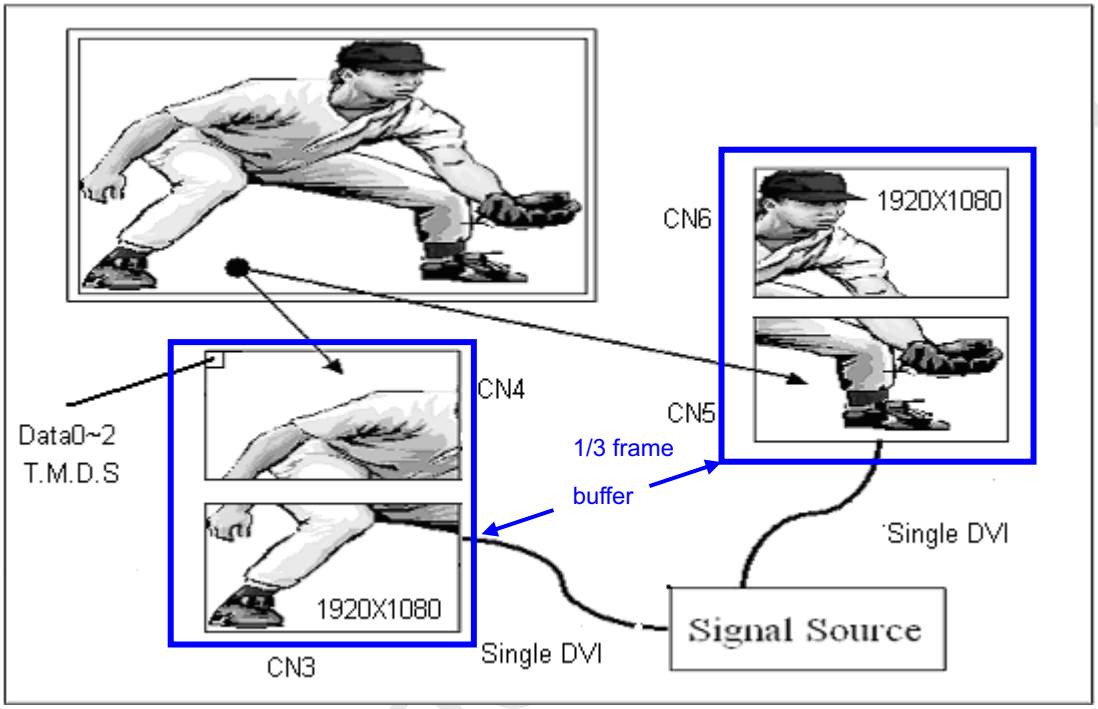
CN3-CN4 (Master, Header), CN5-CN7 (Slave, Header): 528521070 (Molex)

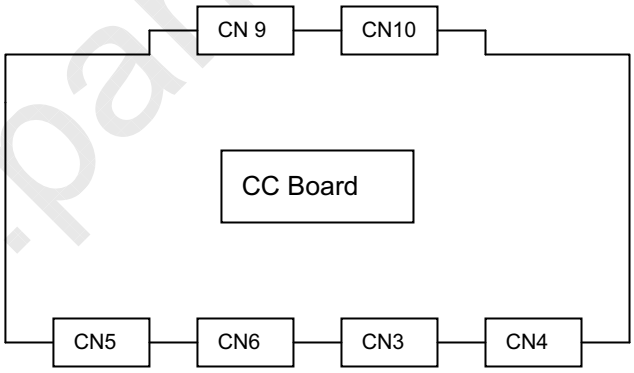
Pin No.	Symbol	Description
1	Control Signal	Board to Board
2		Board to Board
3		Board to Board
4		Board to Board
5		Board to Board
6		Board to Board
7		Board to Board
8		Board to Board
9		Board to Board
10		Board to Board

Note (1) Floating of any control signal is not allowed.

6.5. BLOCK DIAGRAM OF IMAGE SIGNAL

The video picture (3840x2160) should be divided into four parts: the left up side (1920x1080), the left down side (1920x1080), the right up side(1920x1080) and the right down side(1920x1080). Signals of these four parts should be delivered into the module individually through each single-DVI. And the protocol of DVI is specified in the DVI specification of DDWG





Note (1) It must be “synchronous” mutually between signals from CN3 and CN4.

Note (2) It must be “synchronous” mutually between signals from CN5 and CN6.

Note (3) It exists 1/3 frame buffer (i.e. buffer =1/3 x 1920 x1080 pixels) between (CN3/CN4) and (CN5/CN6)

Note (4) Signals of CN4 and CN6 must always be delivered to keep all of the power that’s necessary turned on normally during the operation.

Note (5) “Synchronous” written in (1) and (2) is defined as a time difference smaller than 7 CLKs.

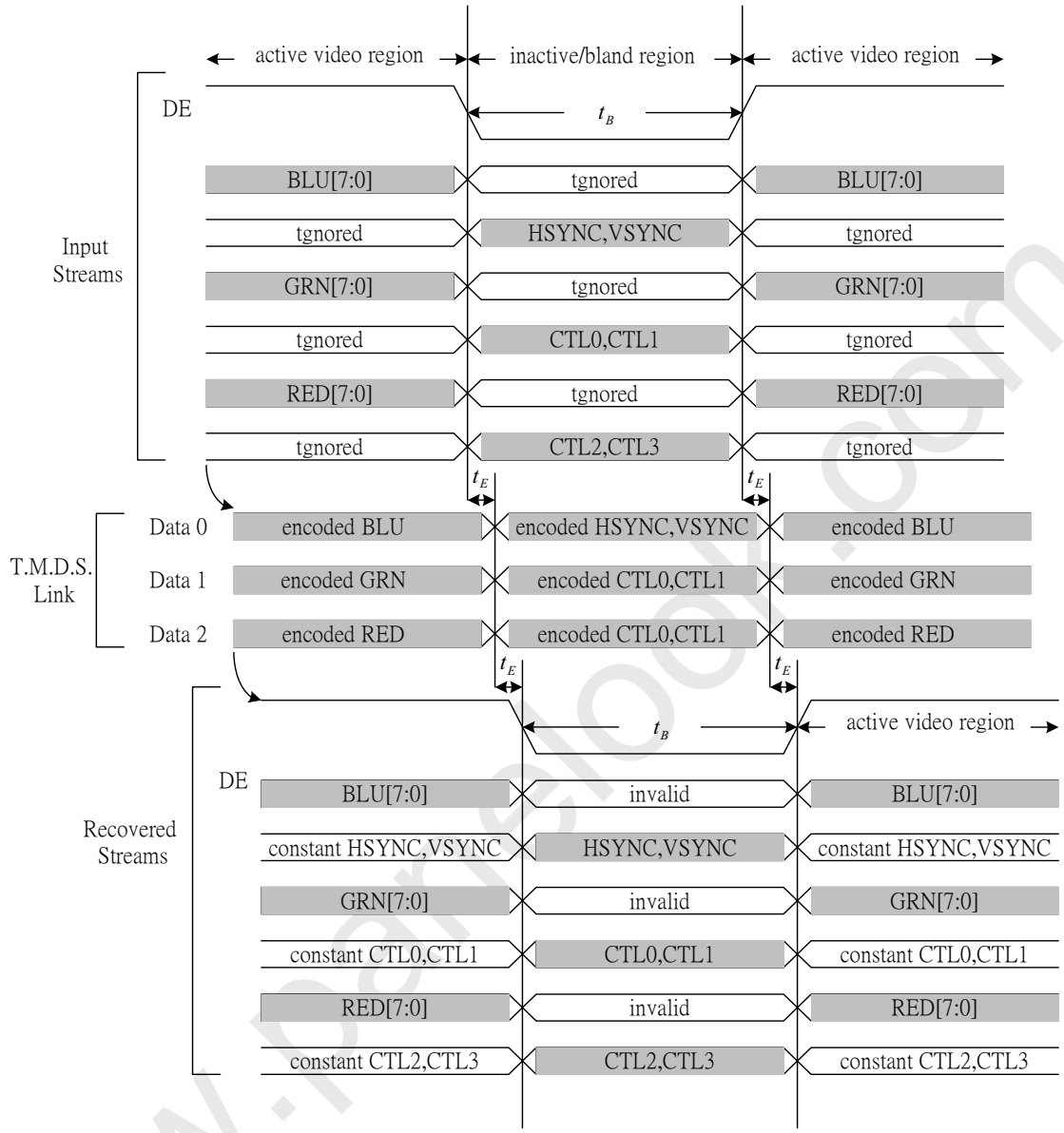
6.6. DVI SIGNAL LIST

Signal Name	Signal Description	Note
T.M.D.S. Signals		
T.M.D.S. Clock + & -	T.M.D.S. clock differential pair.	
T.M.D.S. Clock Shield	Shield for T.M.D.S. clock differential pair.	
T.M.D.S. Data0 + & -	T.M.D.S. link #0 channel #0 differential pair.	
T.M.D.S. Data0/5 Shield	Shared shield for T.M.D.S. link #0 channel #0 and link #1 channel #2.	
T.M.D.S. Data1 + & -	T.M.D.S. link #0 channel #1 differential pair.	
T.M.D.S. Data2/4 Shield	Shared shield for T.M.D.S. link #0 channel #2 and link #1 channel #1.	
T.M.D.S. Data2 + & -	T.M.D.S. link #0 channel #2 differential pair.	
T.M.D.S. Data1/3 Shield	Shared shield for T.M.D.S. link #0 channel #1 and link #1 channel #0.	
T.M.D.S. Data3 + & -	T.M.D.S. link #1 channel #0 differential pair.	
T.M.D.S. Data4 + & -	T.M.D.S. link #1 channel #1 differential pair.	
T.M.D.S. Data5 + & -	T.M.D.S. link #1 channel #2 differential pair.	
Control Signals		
Hot Plug Detect(HPD)	Signal is driven by monitor to enable the system to identify the presence of a monitor.	
DDC Data	The data line for the DDC interface.	
DDC Clock	The clock line for the DDC interface	
+5V Power	+5 volt signal provided by the system to enable the monitor to provide EDID data when the monitor circuitry is not powered.	
Ground (for +5V)	Ground reference for +5 volt power pin. Used as return by Hsync and Vsync Signals.	
Analog Signals		
Analog Red	Analog Red signal.	(1)
Analog Green	Analog Green signal.	
Analog Blue	Analog Blue signal.	
Analog Horizontal Sync	Horizontal synchronization signal for the analog interface.	
Analog Vertical Sync	Vertical synchronization signal for the analog interface.	
Analog Ground	Common ground for analog signals. Used as a return for analog red, green and blue signals only.	

Note (1) No using.

Note (2) The DVI signal list is specified in the DVI specification of DDWG.

6.7. DVI LINK TIMING REQUIREMENTS



Symbol	Description	Value	Unit
t_B	Minimum duration blanking period required to ensure character boundary recovery at the receiver. Blanking periods of this duration must occur at least once every 50mS (20Hz).	128	T_{pixel}
t_E	Maximum encoding/serializer pipeline delay.	64	T_{pixel}
t_R	Maximum recovery/de-serizlizer pipeline delay. Recovery timing includes inter-channel skew, and is measured from the earliest DE transition among the data channels.	64	T_{pixel}

Note: The DVI link timing requirements are specified in the DVI specification of DDWG.

7. TIMING REQUIREMENTS OF IMAGE SIGNAL

7.1. INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

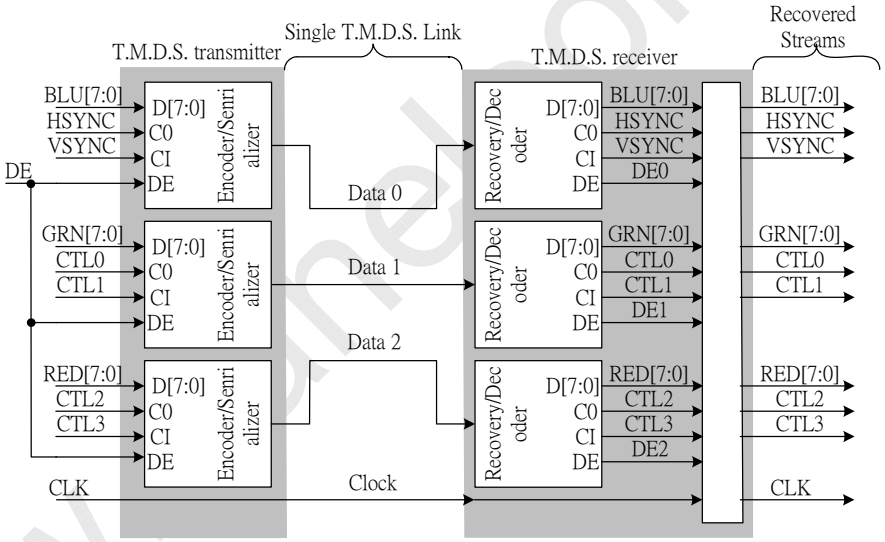
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DVI Receiver Clock (Single DVI)	Frequency	1/Tc	120	144	152	MHz	(1)
Vertical Active Display Term (Single DVI,1920x1080 Active Area)	Frame Rate	Fr5	47	50	53	Hz	(2)
		Fr6	57	60	63	Hz	(3) (4)
	Total	Tv	1082	1090	1150	Th	Tv=Tvd+Tvb
	Display	Tvd	-	1080	-	Th	
	Blank	Tvb	2	10	70	Th	
Horizontal Active Display Term (Single DVI,1920x1080 Active Area)	Total	Th	2190	2200	2350	Tc	Th=Thd+Thb
	Display	Thd	-	1920	-	Tc	
	Blank	Thb	270	280	430	Tc	

Note (1) The value of Typ. is based on 60Hz operation.

Note (2) (ODSEL) = (H). Please refer to Section 6.2 for detail information.

Note (3) (ODSEL) = (L). Please refer to Section 6.2 for detail information.

Note (4) The value of Max. will be modified beyond 60 Hz in the future due to the improvement from design.



Note: The single link T.M.D.S. channel map is specified in the DVI specification of DDWG.

7.2. EXTENDED DISPLAY IDENTIFICATION DADA (EDID) STRUCTURE

Address	No. bytes		Description	Address	No. bytes		Description
00h	8	Bytes	Header	1Ch		1	Red -y
00h		1	00h	1Dh		1	Green -x
01h		1	FFh	1Eh		1	Green -y
02h		1	FFh	1Fh		1	Blue -x
03h		1	FFh	20h		1	Blue -y
04h		1	FFh	21h		1	White -x
05h		1	FFh	22h		1	White -y
06h		1	FFh	23h	3	Bytes	Established Timings
07h		1	00h	23h		1	Established Timings 1
08h	10	Bytes	Vender/Product Identification	24h		1	Established Timings 2
08h		2	ID Manufacturer Name	25h		1	Manufacturers Reserved Timings
0Ah		2	ID Product Code	26h	16	Bytes	Standard Timing Identification
0Ch		4	ID Serial Number	26h		2	Standard Timing Identification #1
10h		1	Week of Manufacture	28h		2	Standard Timing Identification #2
11h		1	Year of Manufacture	2Ah		2	Standard Timing Identification #3
12h	2	Bytes	EDID Structure Version/Revision	2Ch		2	Standard Timing Identification #4
12h		1	Version #	2Eh		2	Standard Timing Identification #5
13h		1	Revision #	30h		2	Standard Timing Identification #6
14h	5	Bytes	Basic Display Parameters/Features	32h		2	Standard Timing Identification #7
14h		1	Video Input Definition	34h		2	Standard Timing Identification #8
15h		1	Max.Horizontal Image Size	36h	72	Bytes	Detailed Timing Descriptions
16h		1	Max.Vertical Image Size	36h		18	Detailed Timing Description #1 or Monitor Descriptor.
17h		1	Display Transfer Characteristic (Gamma)	48h		18	Detailed Timing Description #2 or Monitor Descriptor.
18h		1	Feature Support	5Ah		18	Detailed Timing Description #3 or Monitor Descriptor.
19h	10	Bytes	Color Characteristics	6Ch		18	Detailed Timing Description #4 or Monitor Descriptor.
19h		1	Red / Green Low Bits	7Eh	1	Byte	Extension Flag
1Ah		1	Blue / White Low Bits	7Fh	1	Byte	Checksum
1Bh		1	Red -x				

Note : The EDID structure is specified in the EDID standard of VESA.

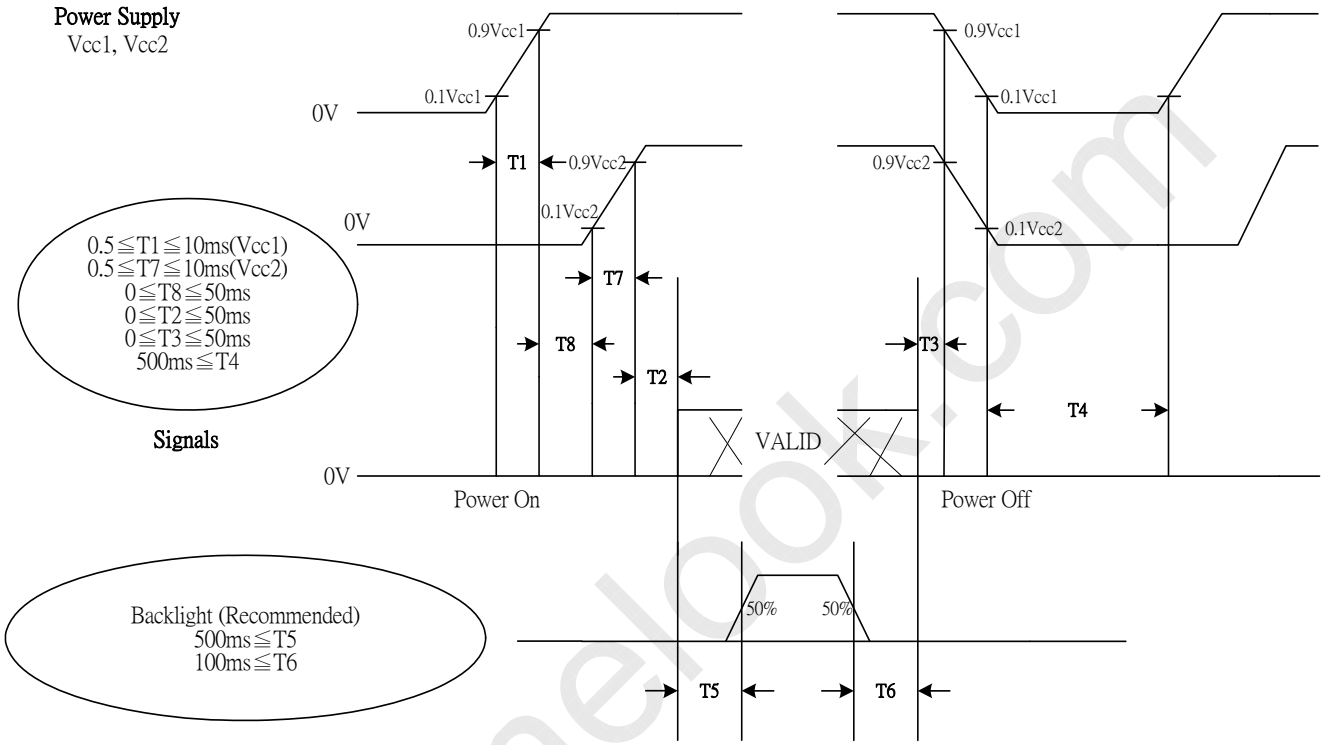
7.3. EXTENDED DISPLAY IDENTIFICATION DADA (EDID) CODE

ADDR	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
000000	00	FF	FF	FF	FF	FF	FF	00	3A	C4	10	A0	64	00	00	00
000010	31	0F	01	03	80	34	21	78	EE	EE	50	A3	54	4C	9B	26
000020	0F	50	54	00	00	00	01	01	01	01	01	01	01	01	01	01
000030	01	01	01	01	01	01	34	38	80	18	71	38	0A	40	10	50
000040	12	00	54	30	34	00	00	18	D6	2E	80	18	71	38	0A	40
000050	10	50	12	00	54	30	34	00	00	18	F6	2C	80	18	71	77
000060	0A	40	10	50	12	00	54	30	34	00	00	18	00	00	00	00
000070	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	38

Note: The EDID code implies 60Hz, 50Hz and 48Hz.

7.4. POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be followed as the diagram below.



Power ON/OFF Sequence

Note (1) The supplied voltage of the external system for the module input should follow the definition of Vcc1,2.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) T4 should be measured after the module being fully discharged between power off and on period.

Note (4) Interface signal shall not be kept at high impedance when the power is on.

8. OPTICAL CHARACTERISTICS

8.1. TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	6.0±0.5	mA
Oscillating Frequency (Inverter)	F_L	50±3	KHz
Frame Rate	F_r	60	Hz

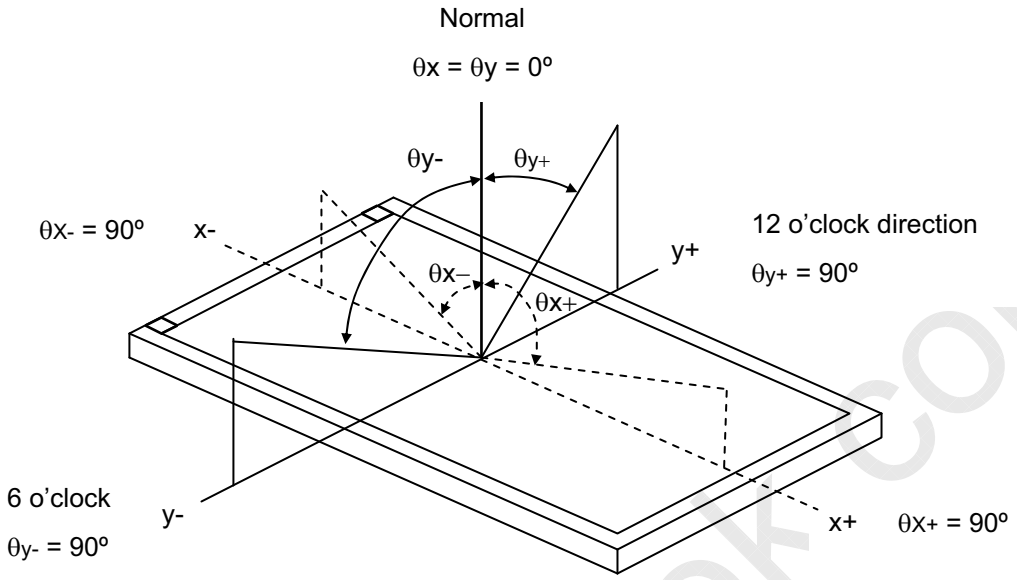
8.2. OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 8.2 Notes. The following items should be measured under the test conditions described in 8.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing angle at normal direction	900	1200		-	Note (2)
Response Time		Gray to gray			6.5		ms	Note (3)
Center Luminance of White		L_C		400	450		cd/m^2	Note (4)
Average Luminance of White		L_{AVE}		400	450		cd/m^2	Note (4)
White Variation		δW				1.6	-	Note (7)
Cross Talk		CT				2	%	Note (5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.651	Typ. +0.03	-	Note (6)
		Ry			0.332		-	
	Green	Gx			0.269		-	
		Gy			0.593		-	
	Blue	Bx			0.144		-	
		By			0.060		-	
	White	Wx			0.285		-	
		Wy			0.293		-	
	Color Gamut	C.G		72	75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥30	80	88		Deg.	Note (1)
		θ_x-		80	88			
	Vertical	θ_Y+		80	88			
		θ_Y-		80	88			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

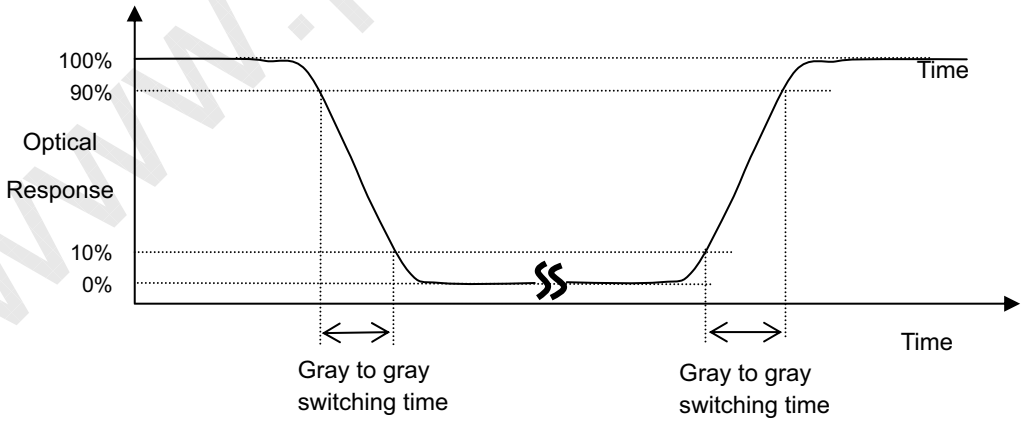
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (7), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time:



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other.

Note (4) Definition of Luminance of White (LC, LAVE):

Measure the luminance of gray level 255 at center point and 5 points

LC = L (7)

LAVE = [L (4)+ L (5)+ L (7)+ L (9)+ L (10)] / 5

Where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

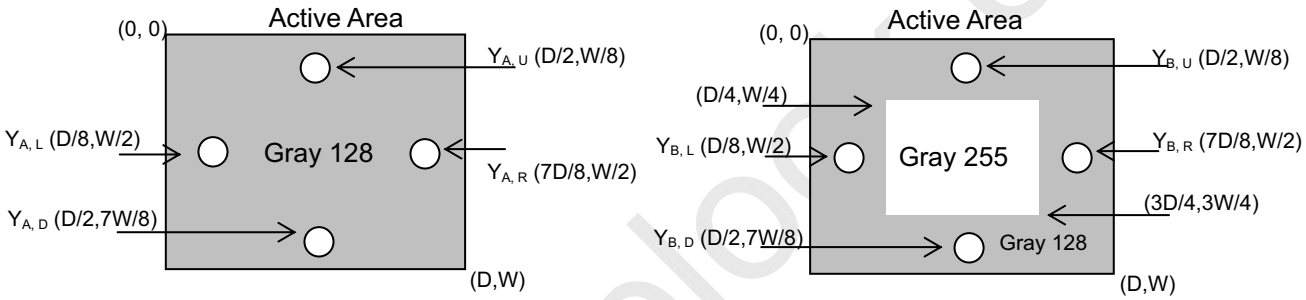
Note (5) Definition of Cross Talk (CT):

CT = | YB – YA | / YA × 100 (%)

Where:

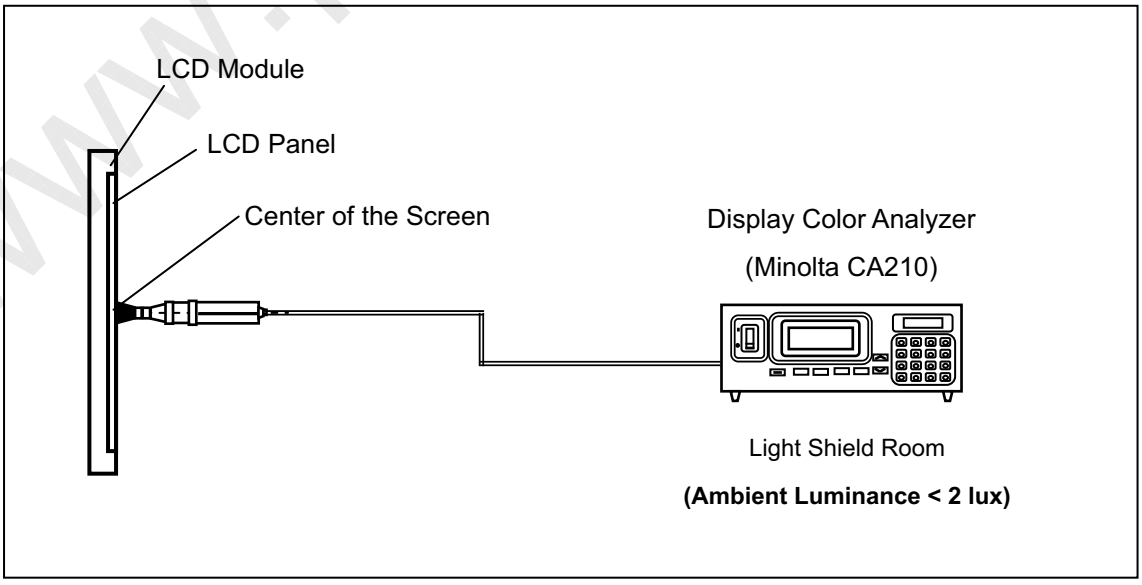
YA = Luminance of measured location without gray level 255 pattern (cd/m2)

YB = Luminance of measured location with gray level 255 pattern (cd/m2)



Note (6) Measurement Setup:

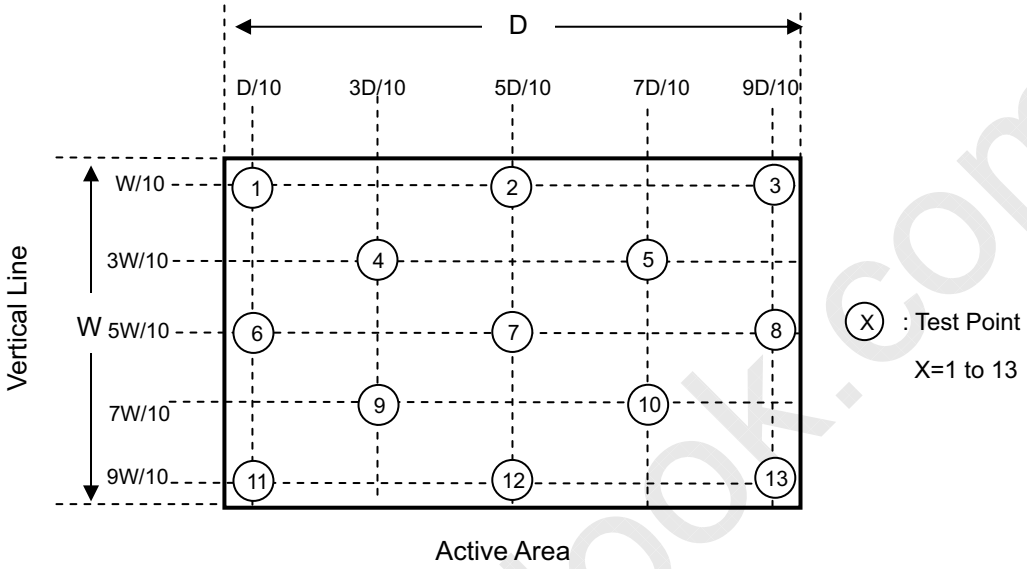
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 128 at 13 points

δW = Maximum [L (1), L (2), L (3), L (4), 、、、, L (13)] / Minimum [L (1), L (2), L (3), L (4), 、、、, L (13)]



9. PRECAUTIONS

9.1. ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) When storing modules as spares for a long time, the following precaution is necessary.

a. Do not leave the module in high temperature, and high humidity for a long time.It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity without condensation.

b. The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

9.2. SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9.3. SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

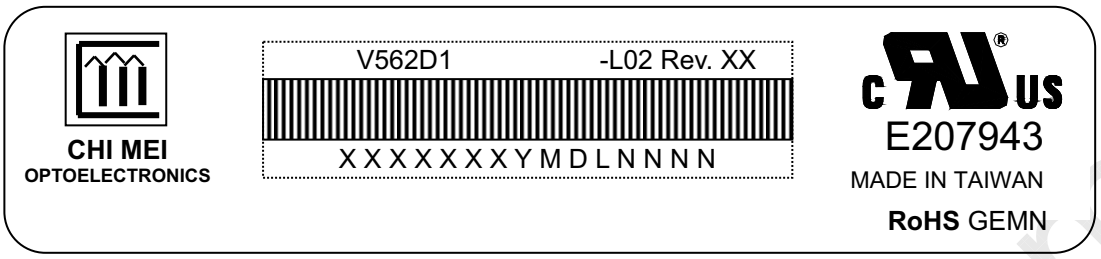
(3) UL60065 or updated standard.

(4) IEC60065 or updated standard.

10. DEFINITION OF LABELS

10.1. CMO MODULE LABEL

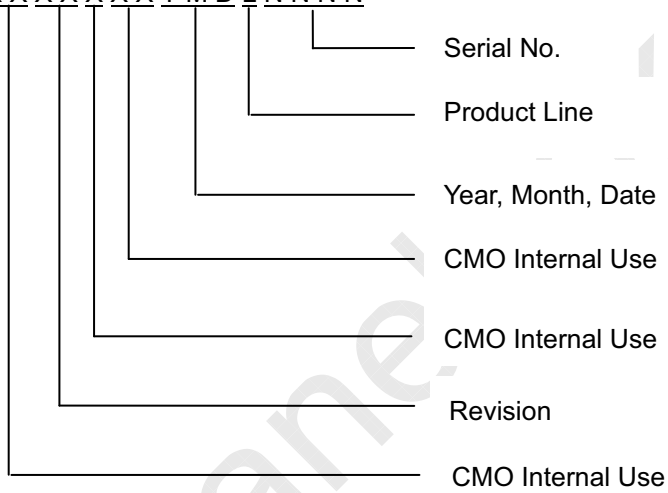
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V562D1-L02

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

(a) Manufactured Date: Year: 0~9, for 2000~2009
Month: 1~9, A~C, for Jan. ~ Dec.
Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

(b) Revision Code: Cover all the change

(c) Serial No.: Manufacturing sequence of product

(d) Product Line: 1 -> Line1, 2 -> Line 2, …etc.

11. PACKAGE

11.1. PACKING SPECIFICATIONS

(1) 2 lcd TV modules / 1 Box

(2) Box dimensions: 1448(L) X 372 (W) X 901 (H)

(3) Weight: approximately 56Kg (2 modules per box)

(4) One protective film is attached on the LCD TV

11.2. PACKING METHOD

Figures 11-1 and 11-2 are the packing method

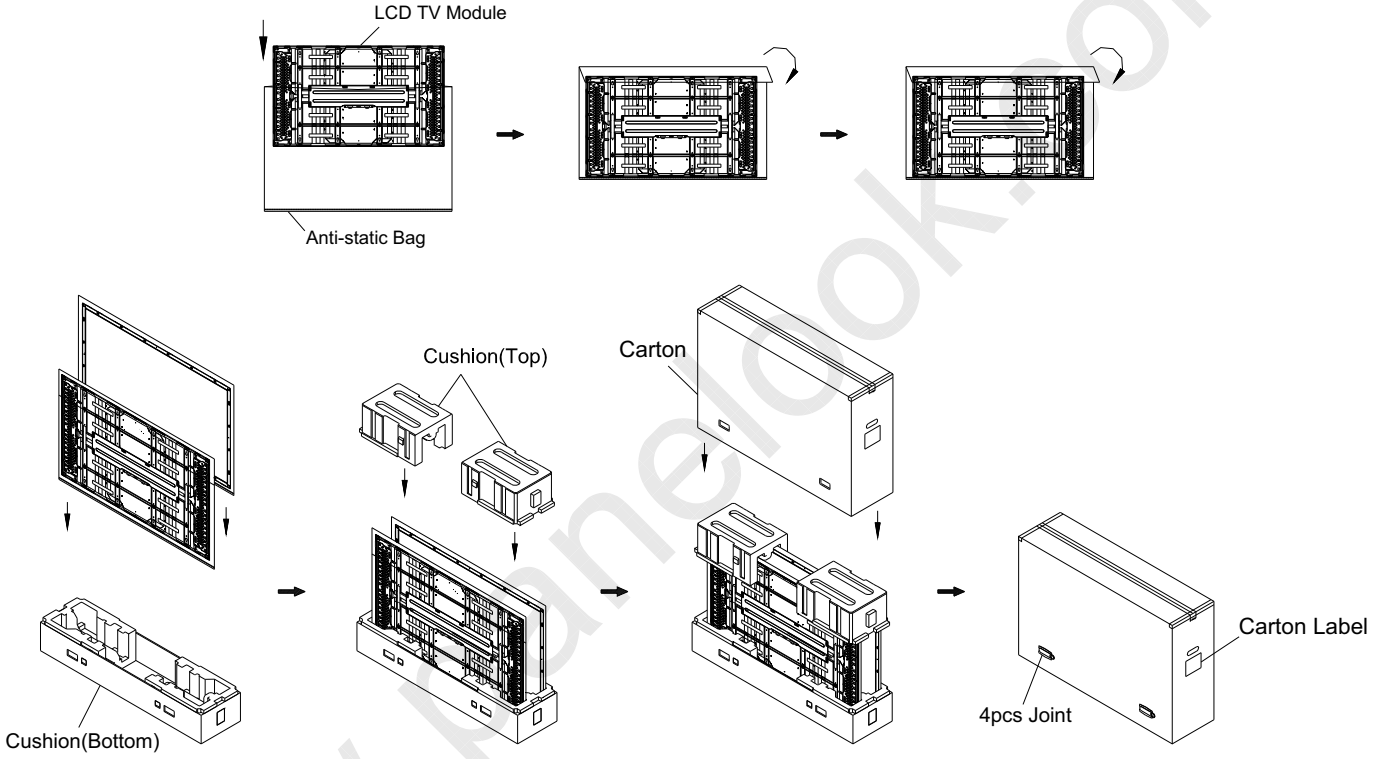
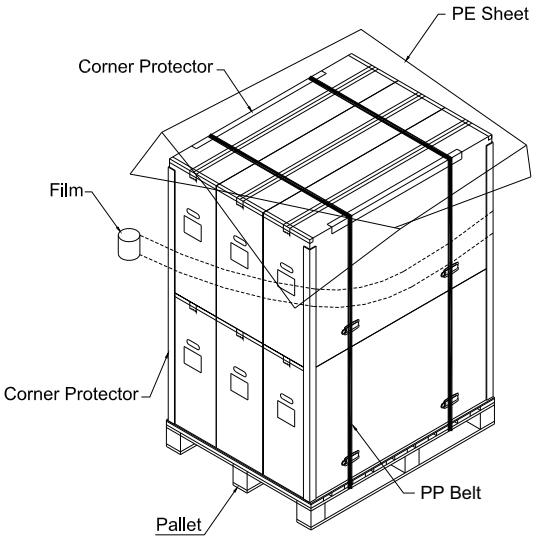


Figure.11-1 packing method

Sea Transportation

Corner Protector:L1780*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1460*H140mm
Pallet Stack:L1150*W1460*H1942mm
Gross:353kg



Air Transportation

Corner Protector:L800*50mm*50mm
Corner Protector:L1130*50mm*50mm
Pallet:L1150*W1460*H140mm
Pallet Stack:L1150*W1460*H1041mm
Gross:185kg

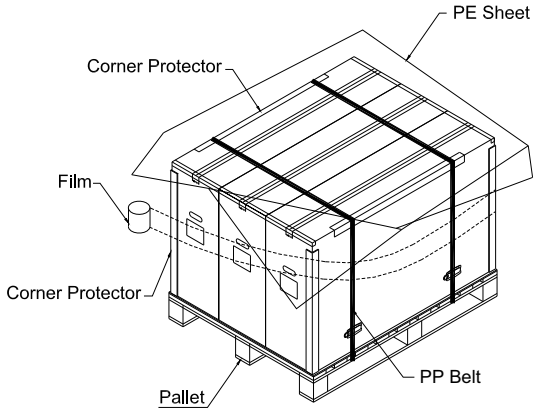


Figure.11-2 Packing method

12. MECHANICAL CHARACTERISTIC